

Study of a new parallel Monte Carlo neutron transport simulation model

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This work presents a hybrid parallel Monte Carlo based neutron transport simulation program which has been developed using the Message-passing Interface (MPI) and the Compute Unified Device Architecture (CUDA) technologies. Such program is supposed to run on a GPU-Cluster, that means, a computer cluster in which the nodes are provided with programmable Graphics Processing Units (GPU). A quite simple but very time consuming Monte Carlo simulation has been considered in order to shown that by making use of an uncomplicated and low cost computer architecture, it is possible to achieve great gains in terms of computational performance. Considering that a standard PC provides no more than few slots for GPUs (commonly 2), and motivated by the gain observed (in Heimlich et al., 2011), the hybrid (GPU/Cluster) proposed in this work is intended to allow for the use of a higher number of GPUs in the solution of a nuclear engineering problem and the simulation of neutron transport through a slab by the Monte Carlo (MC) method. The idea is to use many GPUs located at the nodes (computers) of a cluster. To accomplish that, MPI has been used together with GPU programming techniques (CUDA and Compute Unified Device Architecture). Several programs using MPI and CUDA technologies have been developed by using a cluster comprised by 4 quad-core computers with 2 GPU each. Many experiments using different configurations from 1 to 8 GPUs have been performed and results have been compared with the sequential (non-parallel) version. The best case scenario was: a speedup of more than 2000 times, observed when the 8-GPU was compared with the sequential version. As an example, the proposed method was more than 2000 times faster than the sequential program running on a single processor. Here, the physical model, hardware

and software architecture, as well as the results obtained in comparative experiments are described and commented. Figure 1 shows an example of the parallel hardware architecture.

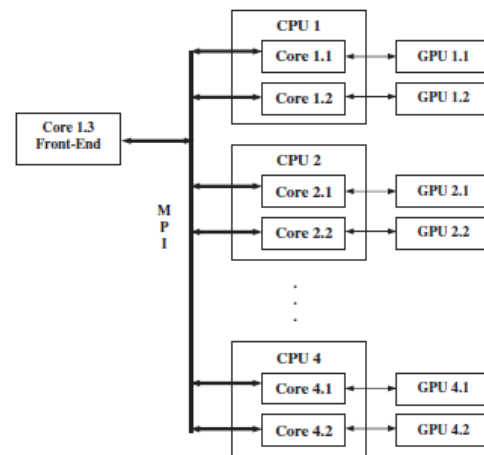


Figure 1. The parallel hardware architecture.

References

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