CMOS switched-capacitor DSB-SSB converter using Hilbert transformer

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Keywords: CMOS integrated circuit, Hilbert transform, switched-capacitor circuit.

This report presents the realization of an analog integrated circuit for conversion of Double-Sideband (DSB) amplitude-modulated signals into Single-Sideband (SSB) [1]. The continuous-time analog DSB input with carrier frequency f_c is demodulated by a coherent amplitude demodulator to obtain the baseband (BB) signal that constitutes the transmitted information. Next, the BB signal is modulated by a Hartley modulator resulting in the SSB output with same amplitude and carrier frequency as the DSB input but only half of its frequency band allocation, doubling the number of possible simultaneous transmitters. The converter is implemented by discrete-time switched-capacitor (SC) circuits and was fully integrated in a 180 nm CMOS technology with metal-metal (MiM) capacitors as shown in Figure 1, totaling 27 operational amplifiers and 916 capacitors. The DSB demodulator consists of a frequency mixer (*mixer* in Figure 1) and a 5th-order low-pass filter (*LP*) to reject spectral images of the DSB input introduced by the mixer above f_c. The Hartley modulator comprises a 90º phase shifter and a quadrature frequency mixer (*qmod*). The phase shifter is implemented by a 7th-order Hilbert transformer (*HT*) with Infinite Impulse Response (IIR). Both *LP* and *HT* are realized by associations of 1st- and 2nd-order structurally all-pass (AP) filters, which greatly reduces the converter's sensitivity to capacitor mismatch. Additionally, in case the sampling frequency f_s equals $8 \cdot f_c$, both frequency mixers can be reduced to simple variable-gain voltage amplifiers and the Hartley modulator's switching frequency can be reduced by half. For 1.8 V power supply and 1 V differential input signals with BB frequency f_{BB} ranging from 25% to 75% of carrier frequency (Figure 2), experimental results show the converter achieves Image Rejection Ratio (IRR) greater than 39.5 dB for Lower-Sideband (LSB) modulation (Figure 3) and 38.0 dB for Upper-Sideband (USB) modulation. Its silicon area is 1.09 mm^2 and the converter consumes only 17.7 mW for 1 MHz sampling frequency while its IRR presents standard deviation of only 0.5 dB among 20 chip samples. The converter's carrier frequency favors the implementation of wireless communications in nuclear facilities since their reinforced building structure turns impractical wireless networks in standard GHz range.

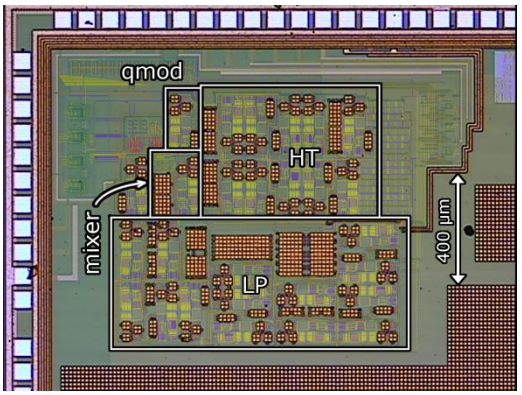

Figure 1.Microphotograph of DSB-SSB converter IC

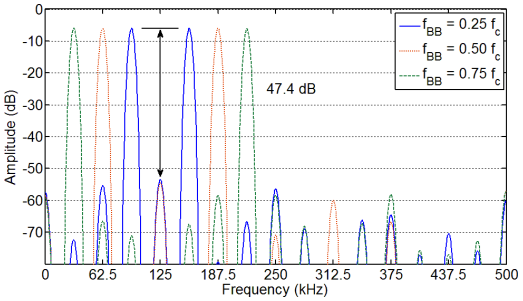

Figure 2. FFT of DSB input for 3 baseband frequencies

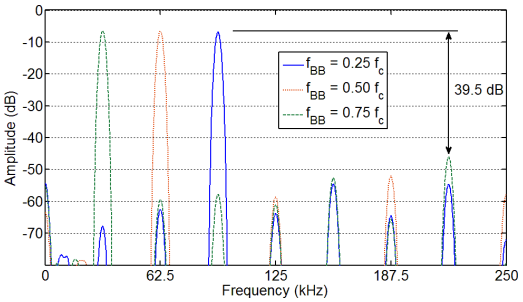

Figure 3. FFT of converter output for LSB modulation

References

[1] LACERDA, F.; PETRAGLIA, A.; GOMES, J. G. R. C. CMOS Switched-capacitor DSB-SSB converter using Hilbert transformer. **IEEE Trans. Circuits Syst. II, Exp. Briefs,** New Jersey, USA, v. PP, n. 99, p. 1-1, 2017.