ARM-based fast sampling of nuclear pulses for multichannel analyzers

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Keywords: ARM processor, multichannel analyzer, pulse sampling, nuclear instrumentation.

In nuclear instrumentation, the energy of an incident radiation can be inferred from the peak level of the electrical pulse produced by a radiation detector. Modern multichannel analyzers (MCAs), capable of evaluating numerous pulses in real time, rely mostly on fast-processing digital technologies such as Field-Programmable Gate Array (FPGA). However, they depend on an Analog-to-Digital Converter (ADC) to transpose the pulse amplitude into the digital domain. Due to the random nature of ionizing radiation over time, the ADC must operate at high sampling rates in order to increase the probability of obtaining at least one sample of each electrical pulse very close to its peak. This report presents a fast pulse sampling solution based on an Advanced RISC Machine (ARM) processor for a MCA currently under development by the authors. Figure 1 shows a photograph of the circuit board containing the ARM processor and Figure 2 illustrates its role within the MCA. The 72-MHz 32-bit ARM processor incorporates an ADC with maximum sampling rate of 4.8 megasamples per second (MSPS) which is suitable for nuclear pulses with Full Width at Half Maximum (FWHM) of 5 µs or more. Since the detector produces nuclear pulses with FWHM not exceeding 1 µs, they are processed by an analog low-pass filter (*FILTER* in Figure 2) to increase their FWHM as well as invert their polarity and match their amplitude to the ADC input range. The filter is preceded by an

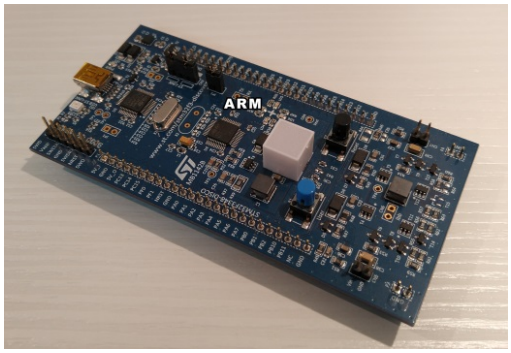

Figure 1. ARM evaluation board

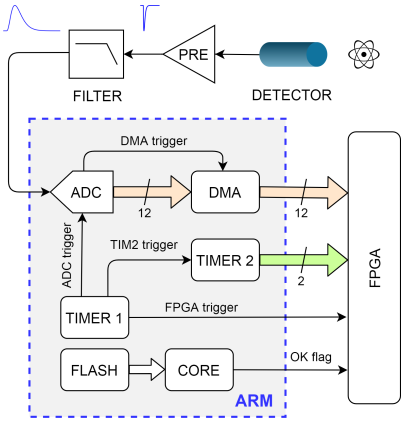

Figure 2. MCA with ARM-controlled nuclear pulse sampling

analog buffer (*PRE*) to isolate the detector from the MCA circuitry. The ARM processor comprises a Cortex-M4 core - which executes software compiled by the design team and stored in its flash memory - along with several peripherals. The core constantly monitors the state of relevant peripherals and signals the FPGA that the system is operational (*OK flag*). ADC sampling rate is defined as 4.8 MSPS by *Timer 1* peripheral (*ADC trigger*). At ADC conversion completion, the *DMA* peripheral is trigged by the ADC (*DMA trigger*) so to output the ADC result to the FPGA via 12 digital pins. Each result is labeled with a 2-bit tag allowing the FPGA to identify missed or duplicated data among adjacent samples. The tag derives from *Timer 2* peripheral, which is also triggered by *Timer 1* (*TIM2 trigger*). Finally, *Timer 1* triggers the FPGA (*FPGA trigger*) once data - ADC result, tag and OK flag - is ready to be received. This procedure is repeated for every ADC conversion. Compared to an MCA employing standalone ADC chips [1], adoption of an ARM processor to supervise ADC conversions proved to be beneficial to the MCA since it increases reliability of the data stream from the ADC to the FPGA even at high transfer rates (> 1 MSPS). Currently the MCA design phase is focused on refining the FPGA algorithm to guarantee no ADC data is missed or misinterpreted as two successive conversions since integrity of the sampling sequence is essential to the MCA's peak detector algorithm.

References

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