Active Redundant Hardware Architecture for Increased Reliability in FPGA-Based Nuclear Reactors Critical Systems

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The hunt for increased reliability in systems for critical applications is a never-ending process and is a point of concern for designers in several different fields, such as nuclear reactors. This concern becomes more prominent when a new device technology is integrated into the options for the development of those systems, such as programmable logic devices like the FPGA. With the constant breakthroughs in this technology, there has been an increase in the capacity and the performance of FPGAs. Nevertheless, new methods to keep fault tolerance at an appropriate level for critical applications in hardware must be considered, particularly due to the transient nature of some radiation-induced faults. This report shows a resilient and adaptable hardware architecture that increases the reliability of circuits implemented in SRAM-based FPGAs, based on a classic active redundancy model, i.e. Triple Modular Redundancy (TMR) with spares. [1].

The use of SRAM-based FPGA in nuclear reactor critical systems should be supported by many fault mitigation techniques. However, in areas with strict regulations, such as nuclear reactors, where not only faults, but also service interruptions are not tolerated, avoiding the use of debugging techniques, such as scrubbing may be important for the technology to be approved by national regulatory agencies. Figure 1 presents an overview of the proposed architecture to the TMR with two spares (TMR/2) redundant model.

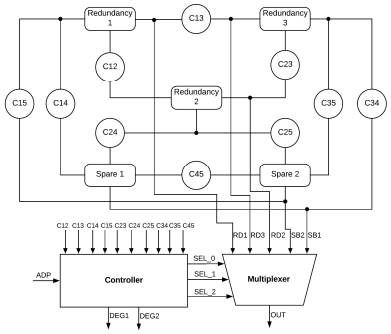

Figure 1. Proposed hardware architecture.

The modules of the redundant TMR/2 used model are Redundancy 1, Redundancy 2, Redundancy 3, Spare 1 and Spare 2. Each of these five components perform the same critical function. The resilient architecture, which receives data from redundant modules and controls the execution of the redundant model, includes ten Comparators, Controller and Multiplexer. Figure 2 allows us to compare the model's reliability. The proposed models (TMR/2 and TMR/1) maintain a higher reliability than the other models during most of the mission time.

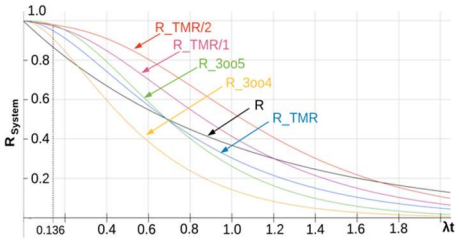

Figure 2. Comparison between the reliability of models.

Table I shows the reliability in percentages of the MTTF (25%, 50% and 75%), respectively with values $\lambda t = 0.25$, $\lambda t = 0.50$ and $\lambda t = 0.75$ to each evaluated model and the proposed models (TMR/1 and TMR/2).

Table I - Comparison between total occupied areas and reliability

Model	Area (LUTs)	Reliability (λt)		
		0.25	0.50	0.75
Simple	378	0.7788	0.6065	0.4724
TMR	1137	0.8731	0.6548	0.4559
3oo4	1515	0.7843	0.4846	0.2706
3oo5	1893	0.9227	0.6910	0.4456
TMR/1	1559	0.9344	0.7783	0.5875
TMR/2	1937	0.9598	0.8626	0.7070

Table I also displays the result of the total area occupied by each model. As can be seen, the occupied area by the TMR/1 model is smaller than 3oo5 model. The results confirm that higher reliability is achieved by the proposed models with less occupied area on the FPGA device.

References

[1] FARIAS, M. S.; NEDJAH, N.; CARVALHO, P. V. R. "Active Redundant Hardware Architecture for Increased Reliability in FPGA-Based Nuclear Reactors Critical Systems," 2020 23rd Euromicro Conference on Digital System Design (DSD), 2020, pp. 608-615, doi: 10.1109/DSD51259.2020.00100.