Efficient hardware architecture for embedded radionuclide identification

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Introduction

The accurate radionuclide identification depends on the ability to determine if specific peaks are present in the spectrum of gamma-emitting sources. Radionuclides are associated to these specific peaks, in which the locations of peaks in the spectrum are used to identify the gamma-ray sources. There are many methods that can be used for automatic radionuclide identification. Most of them are based in software algorithms to peak detection and association to specific peaks. The processing time of these tasks may be too large for applications that require quick responses, such as the use of portable equipment to radionuclide identification. This report describes the hardware implementation (FPGA device) of subtractive clustering algorithm to perform radionuclide identification. The subtractive clustering (SC) was explained in the report *Radionuclide Identification Using Subtractive Clustering*

Proposed architecture

The implementation of subtractive clustering algorithm in hardware is the main point to develop a classification system of radioactive elements. The hardware component showed in the Figure 1 (Component to Subtractive Clustering - CSC) processes all the arithmetic computation to calculate the potential of each point in the subtractive clustering algorithm.

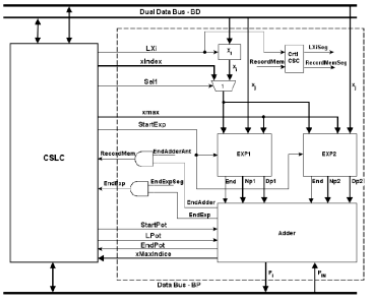

Fig. 1 –The component CSC

It has two components Exp_1 and Exp_2 to compute the exponential value and one component to sum (Adder).

The component CSLC (Component for Storage, Loading and Control) provides to the CSC the set of samples for the selection of cluster centers. The CSLC component works as a main controller of the process based on state machine.

The internal architecture of Exp calculates the exponential value. This value was approximated by a second-order polynomial using the least-squares method. Moreover, this architecture computes these polynomials and all values are represented using fractions [1] as in Equation (1). The proposed architecture allows the CSC to be scaled by adding more of these components in parallel to the computation of the exponential factors [2]. This provides great flexibility to implement the hardware.

$$e^{-\alpha\|x\|} = \frac{N_a}{D_a}\left(\frac{N_v}{D_v}\right)^2 + \frac{N_b}{D_b}\left(\frac{N_v}{D_v}\right) + \frac{N_c}{D_c} \quad (1)$$

Results

The Table 1 shows the application of the SC algorithm running on a MicroBlaze processor to evaluate the processing time in embedded systems.

		Spectrum			
		Ba-133	Eu-152	Cs-137 and Ba-133	Co-60
Number of samples		412	520	775	9654
		Number of cycles x10^3 / Performance gain			
Microblaze		2739587.467	4364128.325	9690870.878	—
Hardware	1 CSC	12959.789 / 211.4	20644.026 / 211.4	45855.467 / 211.3	7115449.045
	2 CSC	6479.890 / 422.8	10322.017 / 422.8	22927.735 / 422.7	3557724.524
	3 CSC	4319.931 / 634.2	6881.344 / 634.2	15285.156 / 634.0	2371816.349
	4 CSC	3239.949 / 845.6	5161.007 / 845.6	11463.867 / 845.3	1778862.262

Table 1 - Cycles required and performance gain.

The performance gain value shows how many times the hardware is faster than the processor to run the algorithm. In this implementation, we used the set of four samples of the spectrum. The results showed that the proposed architecture met the initial goal of designing a hardware that performs efficiently the task of running the SC algorithm for radionuclide identification. These results show that the proposed hardware can be used to develop a portable system for radionuclide identification.

References

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